# IS61C632A

## 32K x 32 SYNCHRONOUS PIPELINED STATIC RAM

### FEATURES

- Fast access time:
  - 4 ns-125 MHZ; 5 ns-100 MHz; 6 ns-83 MHz; 7 ns-75 MHz; 8 ns-66 MHz
- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Power-down control by ZZ input
- JEDEC 100-Pin LQFP and PQFP package
- Single +3.3V power supply
- Two Clock enables and one Clock disable to eliminate multiple bank bus contention.
- Control pins mode upon power-up:
  - MODE in interleave burst mode
  - ZZ in normal operation mode

  These control pins can be connected to GNDQ or VCCQ to alter their power-up state

### DESCRIPTION

The *ICSI* IS61C632A is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, secondary cache for the i486™, Pentium™, 680X0™, and PowerPC™ microprocessors. It is organized as 32,768 words by 32 bits, fabricated with *ICSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

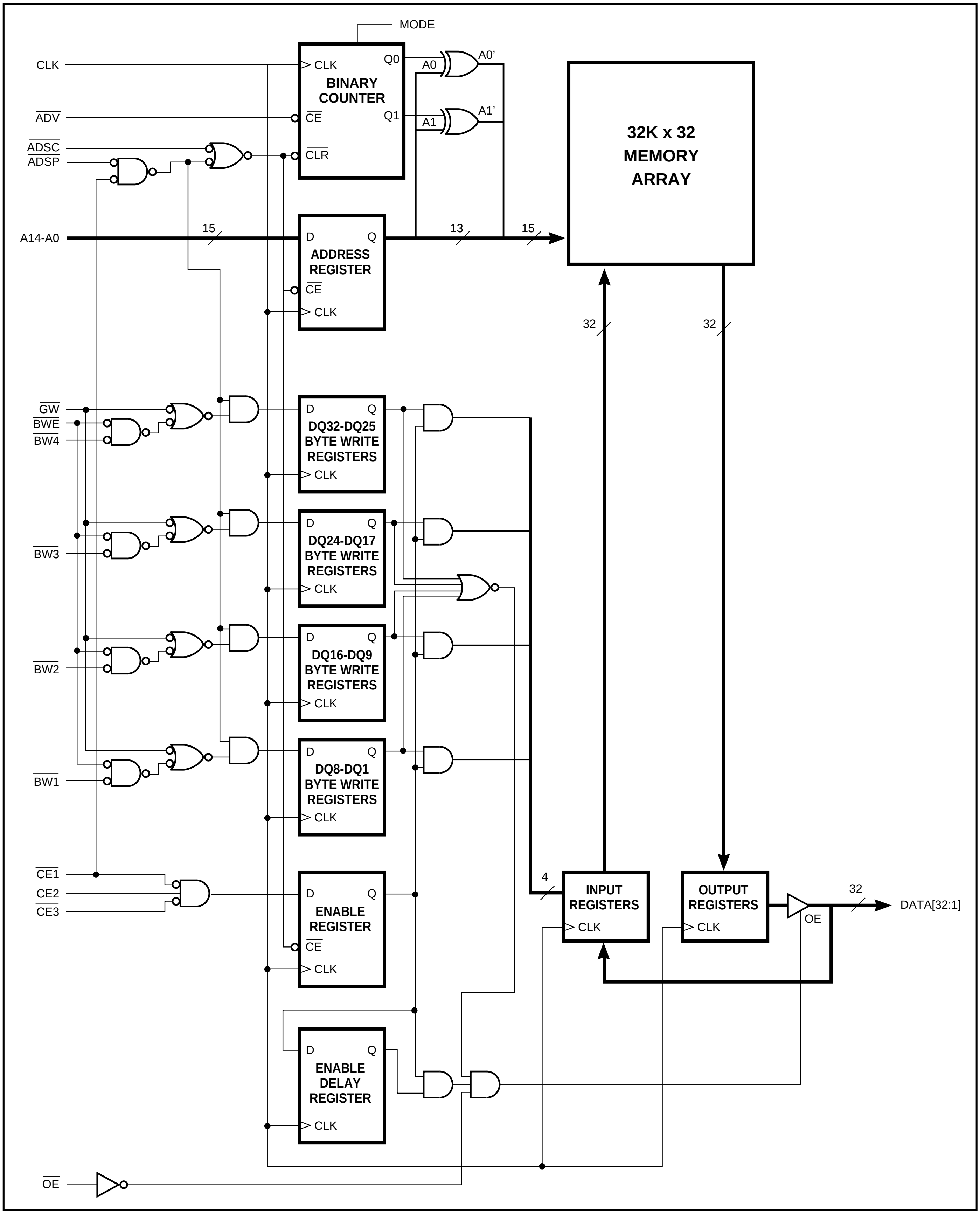
Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8, $\overline{BW2}$ controls DQ9-DQ16, $\overline{BW3}$ controls DQ17-DQ24, $\overline{BW4}$ controls DQ25-DQ32, conditioned by $\overline{BWE}$ being LOW. A LOW on $\overline{GW}$ input would cause all bytes to be written.

Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IS61C632A and controlled by the $\overline{ADV}$ (burst address advance) input pin.

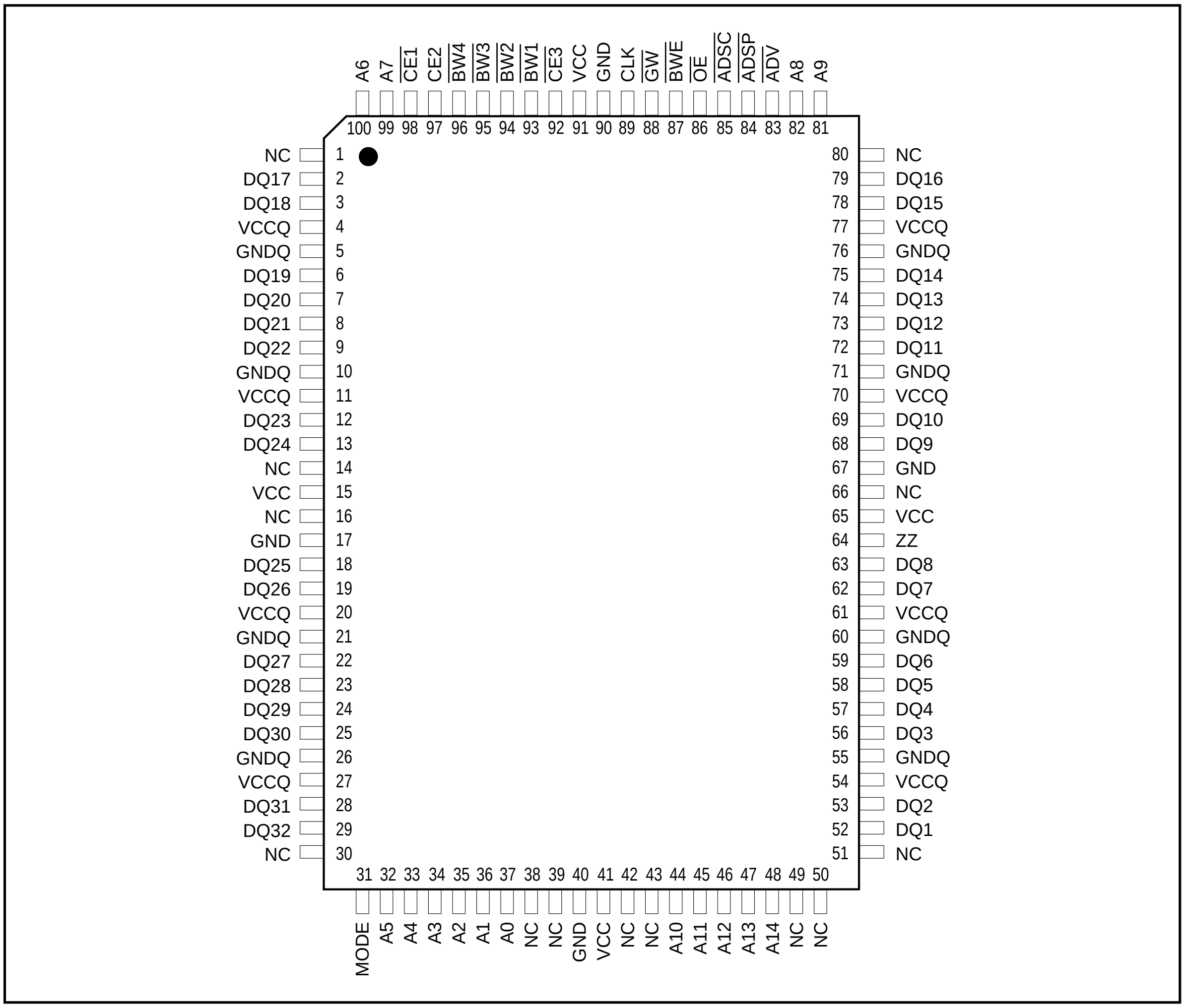
Asynchronous signals include output enable ($\overline{OE}$), sleep mode input (ZZ), clock (CLK) and burst mode input (MODE). A HIGH input on the ZZ pin puts the SRAM in the power-down state. When ZZ is pulled LOW (or no connect), the SRAM normally operates after three cycles of the wake-up period. A LOW input, i.e., GNDQ, on MODE pin selects LINEAR Burst. A VCCQ (or no connect) on MODE pin selects INTERLEAVED Burst.

## BLOCK DIAGRAM



## PIN CONFIGURATION

### 100-Pin LQFP and PQFP (Top View)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A14 | Address Inputs |
| CLK | Clock |
| $\overline{\text{ADSP}}$ | Processor Address Status |
| $\overline{\text{ADSC}}$ | Controller Address Status |
| $\overline{\text{ADV}}$ | Burst Address Advance |
| $\overline{\text{BW1}}$-$\overline{\text{BW4}}$ | Synchronous Byte Write Enable |
| $\overline{\text{BWE}}$ | Byte Write Enable |
| $\overline{\text{GW}}$ | Global Write Enable |
| $\overline{\text{CE1}}$, CE2, $\overline{\text{CE3}}$ | Synchronous Chip Enable |

| | |
|---|---|
| $\overline{\text{OE}}$ | Output Enable |
| DQ1-DQ32 | Data Input/Output |
| ZZ | Sleep Mode |
| MODE | Burst Sequence Mode |
| Vcc | +3.3V Power Supply |
| GND | Ground |
| Vccq | Isolated Output Buffer Supply: +3.3V |
| GNDq | Isolated Output Buffer Ground |

## TRUTH TABLE

| OPERATION | ADDRESS USED | $\overline{CE1}$ | CE2 | $\overline{CE3}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | DQ |
|---|---|---|---|---|---|---|---|---|---|---|
| Deselected, Power-down | None | H | X | X | X | L | X | X | X | High-Z |
| Deselected, Power-down | None | L | L | X | L | X | X | X | X | High-Z |
| Deselected, Power-down | None | L | X | H | L | X | X | X | X | High-Z |
| Deselected, Power-down | None | L | L | X | H | L | X | X | X | High-Z |
| Deselected, Power-down | None | L | X | H | H | L | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | L | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | H | High-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | L | X | D |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | Q |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | H | High-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | Q |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | High-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | Q |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | High-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | D |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | D |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | High-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | High-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | D |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | D |

**Notes:**
1. All inputs except $\overline{OE}$ must meet setup and hold times for the Low-to-High transition of clock (CLK).
2. Wait states are inserted by suspending burst.
3. X means don't care. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$-$\overline{BW4}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
4. For a Write operation following a Read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
5. $\overline{ADSP}$ LOW always initiates an internal READ at the Low-to-High edge of clock. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of clock.

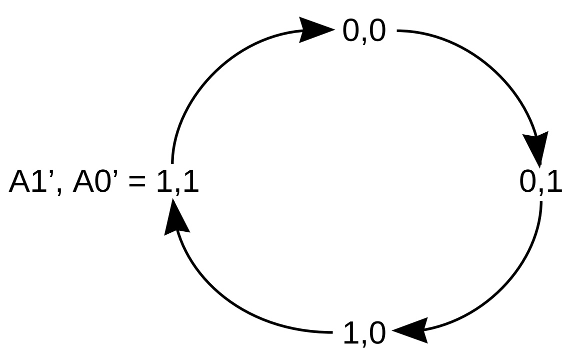
## PARTIAL TRUTH TABLE

| FUNCTION | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW1}$ | $\overline{BW2}$ | $\overline{BW3}$ | $\overline{BW4}$ |
|---|---|---|---|---|---|---|
| READ | H | H | X | X | X | X |
| READ | H | X | H | H | H | H |
| WRITE Byte 1 | H | L | L | H | H | H |
| WRITE All Bytes | X | L | L | L | L | L |
| WRITE All Bytes | L | X | X | X | X | X |

## INTERLEAVED BURST ADDRESS TABLE (MODE = $V_{CCQ}$ or No Connect)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

## LINEAR BURST ADDRESS TABLE (MODE = $GND_Q$)




## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –10 to +85 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +150 | °C |
| $P_D$ | Power Dissipation | 1.8 | W |
| $I_{OUT}$ | Output Current (per I/O) | 100 | mA |
| $V_{IN}$, $V_{OUT}$ | Voltage Relative to GND for I/O Pins | –0.5 to $V_{CCQ}$ + 0.3 | V |
| $V_{IN}$ | Voltage Relative to GND for for Address and Control Inputs | –0.5 to 5.5 | V |

**Notes:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

## OPERATING RANGE

| Range | Ambient Temperature | Vcc |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V +10%, –5% |
| Industrial | –40°C to +85°C | 3.3V +10%, –5% |

## DC ELECTRICAL CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –5.0 mA | | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 5.0 mA | | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage Current | GND ≤ $V_{IN}$ ≤ $V_{CCQ}$[2] | Com.<br>Ind. | –5<br>–10 | 5<br>1- | µA |
| $I_{LO}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CCQ}$, $\overline{OE}$ = $V_{IH}$ | Com.<br>Ind. | –5<br>–10 | 5<br>10 | µA |

## POWER SUPPLY CHARACTERISTICS (Over Operating Range)

| | | | | -4 | | -5 | | -6 | | -7 | | -8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | | Typ. | Max | Typ. | Max. | Typ. | Max. | Typ. | Max. | Typ. | Max. | Unit |
| $I_{CC}$ | AC Operating Supply Current | Device Selected, All Inputs = $V_{IL}$ or $V_{IH}$ $\overline{OE}$ = $V_{IH}$, Cycle Time ≥ $t_{KC}$ min. | Com.<br>Ind. | 150<br>— | 180<br>— | 140<br>— | 170<br>— | 130<br>140 | 160<br>170 | 120<br>130 | 150<br>160 | 110<br>120 | 140<br>150 | mA<br>µA |
| $I_{SB}$ | Standby Current | Device Deselected, $V_{CC}$ = Max., All Inputs = $V_{IH}$ or $V_{IL}$ CLK Cycle Time ≥ $t_{KC}$ min. | Com.<br>Ind. | 15<br>— | 45<br>— | 15<br>— | 45<br>— | 15<br>20 | 45<br>50 | 15<br>20 | 45<br>50 | 15<br>20 | 45<br>50 | mA<br>µA |
| $I_{ZZ}$ | Power-Down Mode Current | ZZ = $V_{CCQ}$, CLK Running All Inputs ≤ GND + 0.2V or ≥ $V_{CC}$ – 0.2V | Com.<br>Ind. | 1<br>— | 10<br>— | 1<br>— | 10<br>— | 1<br>2 | 10<br>20 | 1<br>2 | 10<br>20 | 1<br>2 | 10<br>20 | mA<br>mA |

Note:
1. MODE pin has an internal pull-up. ZZ pin has an internal pull-down. These pins may be a No Connect, tied to GND, or tied to $V_{CCQ}$.
2. MODE pin should be tied to Vcc or GND. They exhibit ±10 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ Vcc – 0.2V.

## CAPACITANCE[1,2]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Input/Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, Vcc = 3.3V.

## AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

## AC TEST LOADS

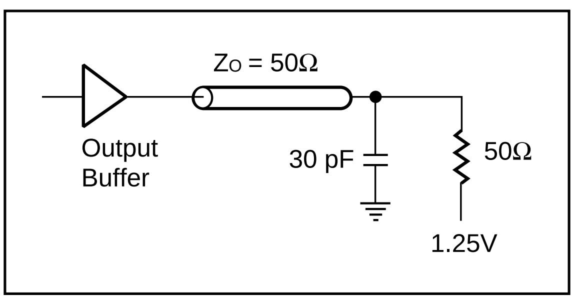



**Figure 1**

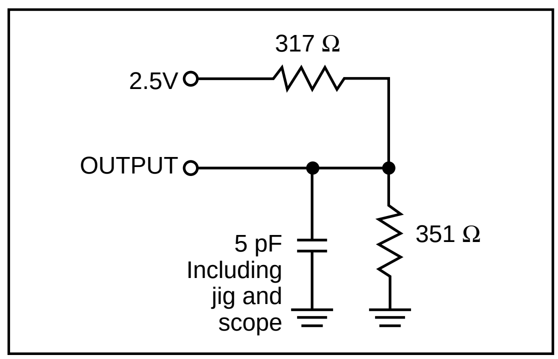


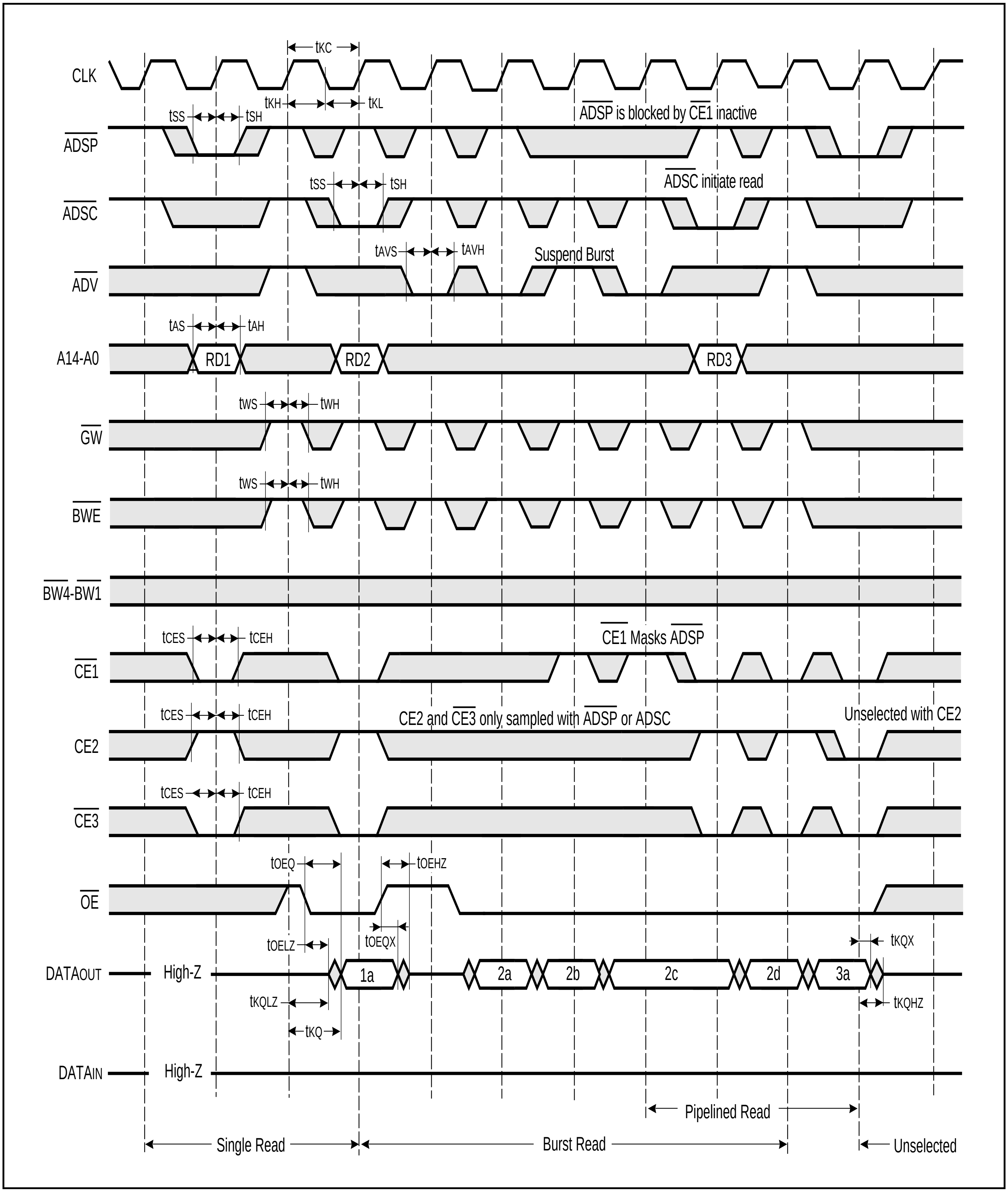

**Figure 2**

## READ CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| | | -4 | | -5 | | -6 | | -7 | | -8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| $t_{KC}$ | Cycle Time | 8 | — | 10 | — | 12 | — | 13 | — | 15 | — | ns |
| $t_{KH}$ | Clock High Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KL}$ | Clock Low Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KQ}$ | Clock Access Time | — | 4 | — | 5 | — | 6 | — | 7 | — | 8 | ns |
| $t_{KQX}$[2] | Clock High to Output Invalid | 1.5 | — | 1.5 | — | 2 | — | 2 | — | 2 | — | ns |
| $t_{KQLZ}$[2,3] | Clock High to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{KQHZ}$[2,3] | Clock High to Output High-Z | 1.5 | 4 | 1.5 | 5 | 2 | 6 | 2 | 6 | 2 | 6 | ns |
| $t_{OEQ}$ | Output Enable to Output Valid | — | 4 | — | 5 | — | 6 | — | 6 | — | 6 | ns |
| $t_{OEQX}$[2] | Output Disable to Output Invalid | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OELZ}$[2,3] | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OEHZ}$[2,3] | Output Disable to Output High-Z | — | 4.5 | — | 4.8 | — | 6 | — | 6 | — | 6 | ns |
| $t_{AS}$ | Address Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{SS}$ | Address Status Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{WS}$ | Write Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{CES}$ | Chip Enable Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{AVS}$ | Address Advance Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{AH}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SH}$ | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{WH}$ | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CEH}$ | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{AVH}$ | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CFG}$ | Configuration Setup[1] | 25 | — | 35 | — | 45 | — | 66.7 | — | 80 | — | ns |

**Notes:**
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with the load in Figure 2.

## READ CYCLE TIMING

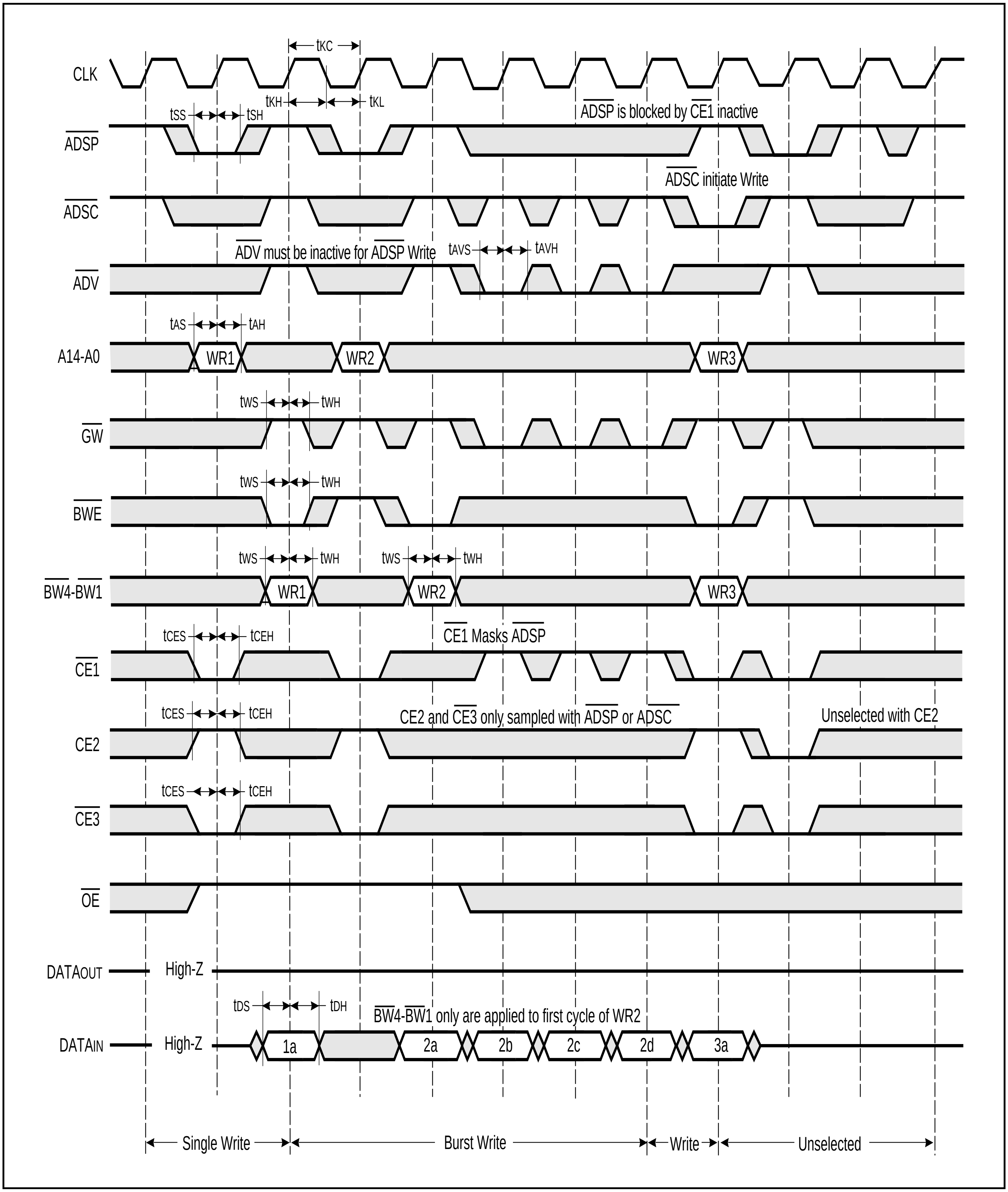


## WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | -4 Min. | -4 Max. | -5 Min. | -5 Max. | -6 Min. | -6 Max. | -7 Min. | -7 Max. | -8 Min. | -8 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{KC}$ | Cycle Time | 8 | — | 10 | — | 12 | — | 13 | — | 15 | — | ns |
| $t_{KH}$ | Clock High Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KL}$ | Clock Low Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{AS}$ | Address Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{SS}$ | Address Status Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{WS}$ | Write Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{DS}$ | Data In Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{CES}$ | Chip Enable Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{AVS}$ | Address Advance Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{AH}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SH}$ | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{DH}$ | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{WH}$ | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CEH}$ | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{AVH}$ | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CFG}$ | Configuration Setup[1] | 25 | — | 35 | — | 45 | — | 52 | — | 60 | — | ns |

**Notes:**
1. Configuration signal MODE is static and must not change during normal operation.

## WRITE CYCLE TIMING

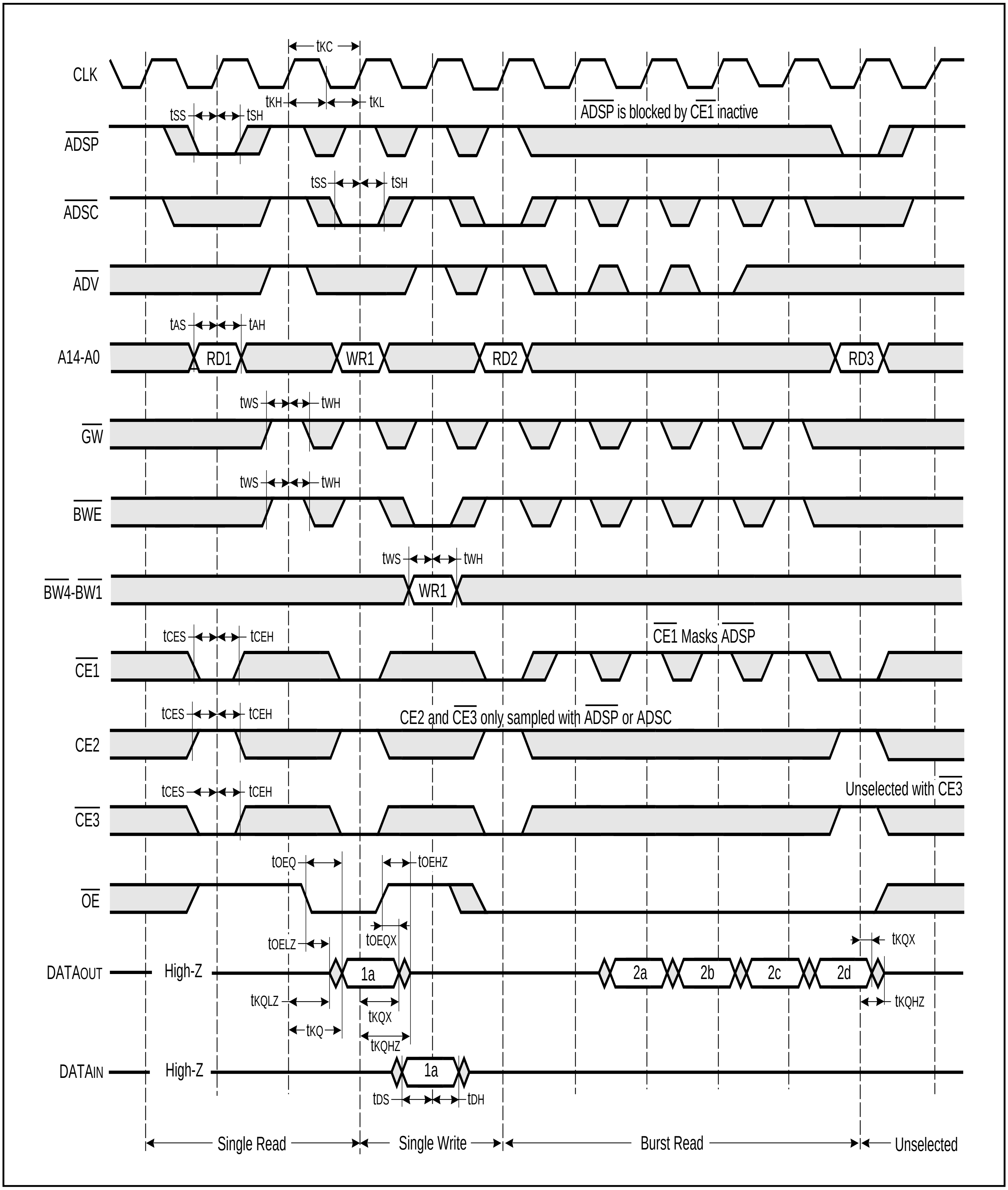


## READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| | | -4 | | -5 | | -6 | | -7 | | -8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| $t_{KC}$ | Cycle Time | 8 | — | 10 | — | 12 | — | 13 | — | 15 | — | ns |
| $t_{KH}$ | Clock High Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KL}$ | Clock Low Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KQ}$ | Clock Access Time | — | 4 | — | 5 | — | 6 | — | 7 | — | 8 | ns |
| $t_{KQX}$(2) | Clock High to Output Invalid | 1.5 | — | 1.5 | — | 2 | — | 2 | — | 2 | — | ns |
| $t_{KQLZ}$(2,3) | Clock High to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{KQHZ}$(2,3) | Clock High to Output High-Z | 1.5 | 4 | 1.5 | 5 | 2 | 6 | 2 | 6 | 2 | 6 | ns |
| $t_{OEQ}$ | Output Enable to Output Valid | — | 4.5 | — | 4.8 | — | 6 | — | 6 | — | 6 | ns |
| $t_{OEQX}$(2) | Output Disable to Output Invalid | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OELZ}$(2,3) | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OEHZ}$(2,3) | Output Disable to Output High-Z | — | 4.5 | — | 4.8 | — | 6 | — | 6 | — | 6 | ns |
| $t_{AS}$ | Address Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{SS}$ | Address Status Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{WS}$ | Write Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{CES}$ | Chip Enable Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{AH}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SH}$ | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{WH}$ | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CEH}$ | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CFG}$ | Configuration Setup(1) | 25 | — | 35 | — | 45 | — | 52 | — | 60 | — | ns |

**Notes:**
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with the load in Figure 2.

## READ/WRITE CYCLE TIMING

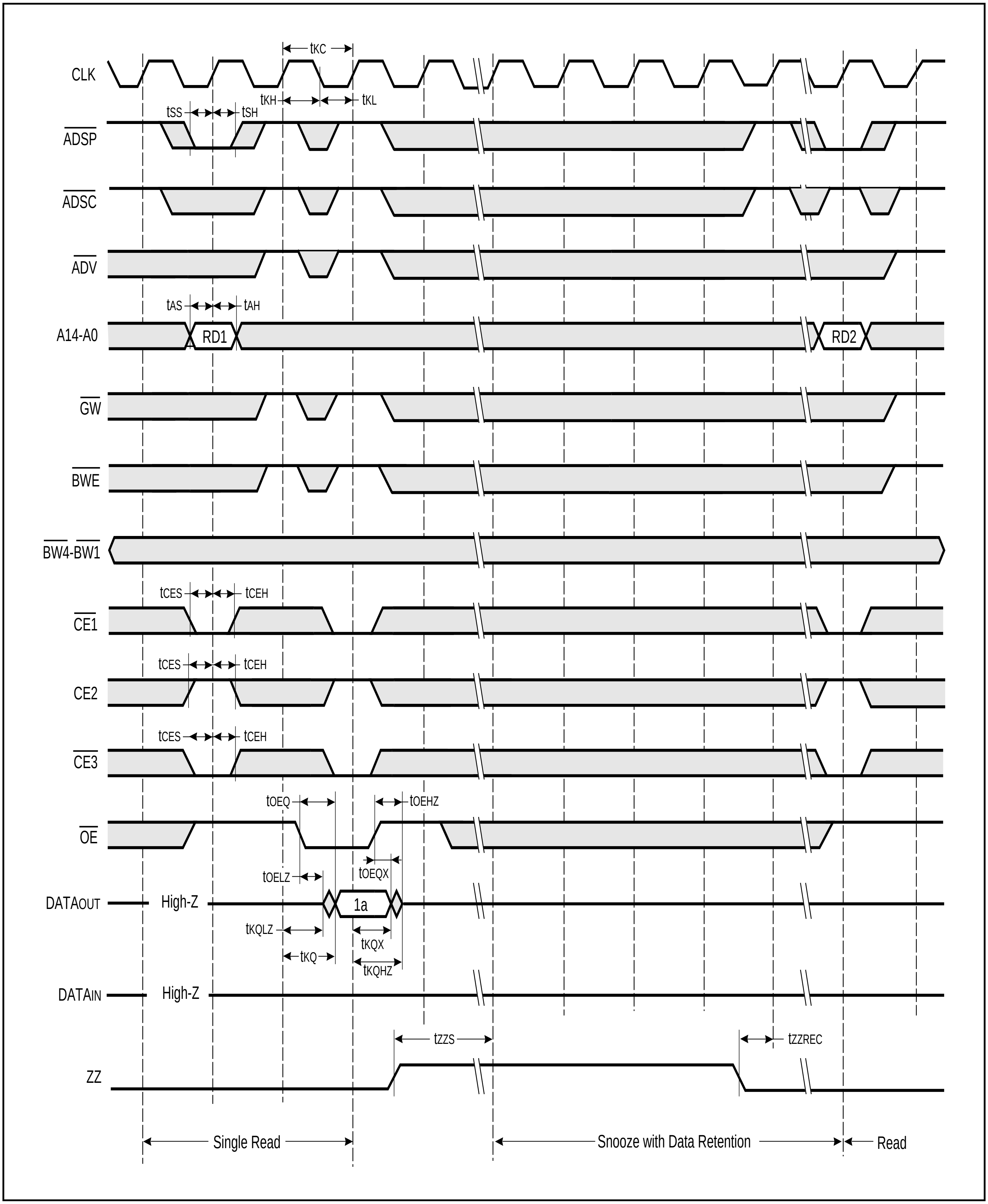


## SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| | | -4 | | -5 | | -6 | | -7 | | -8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| $t_{KC}$ | Cycle Time | 8 | — | 10 | — | 12 | — | 13 | — | 15 | — | ns |
| $t_{KH}$ | Clock High Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KL}$ | Clock Low Time | 4 | — | 4 | — | 4 | — | 6 | — | 6 | — | ns |
| $t_{KQ}$ | Clock Access Time | — | 4 | — | 5 | — | 6 | — | 7 | — | 8 | ns |
| $t_{KQX}$[4] | Clock High to Output Invalid | 1.5 | — | 1.5 | — | 2 | — | 2 | — | 2 | — | ns |
| $t_{KQLZ}$[4,5] | Clock High to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{KQHZ}$[4,5] | Clock High to Output High-Z | 1.5 | 4 | 1.5 | 5 | 2 | 6 | 2 | 6 | 2 | 6 | ns |
| $t_{OEQ}$ | Output Enable to Output Valid | — | 4.5 | — | 5 | — | 6 | — | 6 | — | 6 | ns |
| $t_{OEQX}$[4] | Output Disable to Output Invalid | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OELZ}$[4,5] | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OEHZ}$[4,5] | Output Disable to Output High-Z | — | 4.5 | — | 4.8 | — | 6 | — | 6 | — | 6 | ns |
| $t_{AS}$ | Address Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{SS}$ | Address Status Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{CES}$ | Chip Enable Setup Time | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| $t_{AH}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{SH}$ | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{CEH}$ | Chip Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{ZZS}$ | ZZ Standby[1] | 2 | — | 2 | — | 2 | — | 2 | — | 2 | — | cyc |
| $t_{ZZREC}$ | ZZ Recovery[2] | 2 | — | 2 | — | 2 | — | 2 | — | 2 | — | cyc |
| $t_{CFG}$ | Configuration Setup[3] | 25 | — | 35 | — | 45 | — | 52 | — | 60 | — | ns |

**Notes:**
1. The assertion of ZZ allows the SRAM to enter a lower power state than when deselected within the time specified. Data retention is guaranteed when ZZ is asserted and clock remains active.
2. $\overline{\text{ADSC}}$ and $\overline{\text{ADSP}}$ must not be asserted for at least 2 cyc after leaving ZZ state.
3. Configuration signal MODE is static and must not change during normal operation.
4. Guaranteed but not 100% tested. This parameter is periodically sampled.
5. Tested with the load in Figure 2.

## SNOOZE AND RECOVERY CYCLE TIMING



## ORDERING INFORMATION

### Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part Number | Package |
|---|---|---|
| 4 | IS61C632A-4TQ | 14*20*1.4mm LQFP |
| 4 | IS61C632A-4PQ | 14*20*2.7mm PQFP |
| 5 | IS61C632A-5TQ | 14*20*1.4mm LQFP |
| 5 | IS61C632A-5PQ | 14*20*2.7mm PQFP |
| 6 | IS61C632A-6TQ | 14*20*1.4mm LQFP |
| 6 | IS61C632A-6PQ | 14*20*2.7mm PQFP |
| 7 | IS61C632A-7TQ | 14*20*1.4mm LQFP |
| 7 | IS61C632A-7PQ | 14*20*2.7mm PQFP |
| 8 | IS61C632A-8TQ | 14*20*1.4mm LQFP |
| 8 | IS61C632A-8PQ | 14*20*2.7mm PQFP |

### Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part Number | Package |
|---|---|---|
| 6 | IS61C632A-6TQI | 14*20*1.4mm LQFP |
| 6 | IS61C632A-6PQI | 14*20*2.7mm PQFP |
| 7 | IS61C632A-7TQI | 14*20*1.4mm LQFP |
| 7 | IS61C632A-7PQI | 14*20*2.7mm PQFP |
| 8 | IS61C632A-8TQI | 14*20*1.4mm LQFP |
| 8 | IS61C632A-8PQI | 14*20*2.7mm PQFP |

***Integrated Circuit Solution Inc.***
HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.
TEL: 886-3-5780333
Fax: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.
TEL: 886-2-26962140
FAX: 886-2-26962252
**http://www.icsi.com.tw**